



Handbook of 3D Integration, Volume 3: 3D Process Technology

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Edited by key figures in 3D integration and written by top authors from high-tech companies and renowned research institutions, this book covers the intricate details of 3D process technology. As such, the main focus is on silicon via formation, bonding and debonding, thinning, via reveal and backside processing, both from a technological and a materials science perspective. The last part of the book is concerned with assessing and enhancing the reliability of the 3D integrated devices, which is a prerequisite for the large-scale implementation of this emerging technology.

Invaluable reading for materials scientists, semiconductor physicists, and those working in the semiconductor industry, as well as IT and electrical engineers.

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Editorial Review

From the Back Cover

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Philip Garrou is a consultant and expert witness in the field of IC packaging materials and applications, prior to which he was Dir. of Technology and Business Dev. for Dow Chemicals' Electronic Materials business. Dr. Garrou is a Fellow of IEEE and IMAPS and served as President of the IEEE CPMT Society and IMAPS. He has co-authored 3 microelectronics texts and 100+ publications. He is Assoc. Ed. and author of the weekly blog "Insights from the Leading Edge" for Solid State Technology and has co-authored 3DIC reports for both TechSearch and Yole.

Mitsumasa Koyanagi is Professor in the Graduate School of Engineering at Tohoku University, Japan. After his PhD in electrical engineering he joined the Central Research Laboratory of Hitachi where he was engaged in the research on semiconductor memories. After a three-year stay at the Xerox Palo Alto Research Center in California, USA, he became Professor in the Research Center for Integrated Systems at Hiroshima University, Japan. Mitsumasa Koyanagi received numerous awards, including the Solid-State Devices and Materials Award.

Peter Ramm is head of the department Heterogeneous System Integration of Fraunhofer EMFT in Munich, Germany, where he is responsible for the key competence "Si Processes, Device and 3D Integration". He received the physics and Dr. rer. nat. degrees from the University of Regensburg and subsequently worked for Siemens in the DRAM facility where he was responsible for the process integration. In 1988 he joined Fraunhofer IFT in Munich, focusing for more than 25 years on 3D integration technologies. Peter Ramm is co-author of over 100 publications and 24 patents and editor of Wiley's "Handbook of Wafer Bonding". He received the "Ashman Award 2009" from IMAPS "For Pioneering Work on 3D IC Stacking and Integration".

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