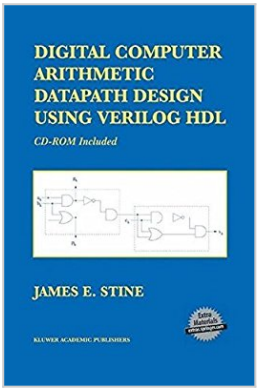

Digital Computer Arithmetic Datapath Design Using Verilog HDL

By James E. Stine

Digital Computer Arithmetic Datapath Design Using Verilog HDL By James E. Stine

This text presents basic implementation strategies for arithmetic datapath designs and methodologies utilized in the digital system. The author implements various datapath designs for addition, subtraction, multiplication, and division. Theory is presented to illustrate and explain why certain designs are chosen. Each implementation is discussed in terms of design choices and how particular theory is invoked in the hardware. Along with the theory that emphasizes the design in question, Verilog modules are presented for understanding the basic ideas that accompany each design. Structural models are implemented to guarantee correct synthesis and for incorporation into VLSI schematic-capture programs. From the modules, the reader can easily add or modify existing code to study current areas of research in the area of computer arithmetic. The emphasis is on the arithmetic algorithm and not the circuit. For any design, both algorithmic and circuit trade-offs should be adhered to when a design is under consideration. Therefore, the idea is to implement each design at the RTL level so that it may be possibly implemented in many different ways (i.e. standard-cell or custom-cell). Thus, professionals, researchers, students, and those generally interested in computer arithmetic can understand how arithmetic datapath elements are designed and implemented. Also included is a CD-ROM which contains the files discussed in the book. The CD-ROM includes additional files utilized in preparing the designs in Verilog including scripts to automatically generate Verilog code for parallel carry-save and tree multipliers. Each Verilog design also contains each module including testbenches to facilitate testing and verification.

Note: The Kindle edition of this book does not include any CDs or DVDs.

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